Claims

1. A SRAM cell, comprising:

first and second internal PMOS transistors; and

first and second internal NMOS transistors,

wherein the first internal PMOS transistor is coupled to the first internal NMOS transistor and the second internal PMOS transistor is coupled to the second internal NMOS transistor, and wherein each internal transistor includes,

a substrate,

a bottom gate disposed on the substrate,

a high resistivity layer disposed on the substrate,

a channel disposed above the bottom gate,

a source disposed on the high resistivity layer and having a source extension extending from a main body of the source and coupled to the channel,

a drain disposed on the high resistivity layer and having a drain extension extending from a main body of the drain and coupled to the channel,

a gate insulator disposed on the channel,

a top gate disposed on the gate insulator,

a first insulating spacer disposed between the top gate and the source and proximate to the source extension, and

a second insulating spacer disposed between the top gate and the drain and proximate to the drain extension.

2. The SRAM cell of claim 1, wherein the channel has a cross-sectional U-shape.

3. The SRAM cell of claim 2, wherein the gate insulator has a cross-sectional U-shape.

4. The SRAM cell of claim 1, wherein each internal NMOS transistor further comprises:

a first local interconnect coupled to the top gate; and

a second local interconnect, insulated from the first local interconnect, and coupled to ground and to the bottom gate.

5. The SRAM cell of claim 1, wherein each internal PMOS transistor further comprises:

a first local interconnect coupled to the top gate; and

a second local interconnect, insulated from the first local interconnect, and coupled to a Vdd source and to the bottom gate.

6. The SRAM cell of claim 1, wherein each internal transistor further comprises a local interconnect coupled to the top gate and insulated from the bottom gate.

7. The SRAM cell of claim 1, wherein each internal transistor further comprises a local interconnect coupled to the top gate and coupled to the bottom gate.

8. A SRAM cell, comprising:

a first internal PMOS transistor coupled to Vdd and a first node;

a second internal PMOS transistor coupled to Vdd and a second node;

a first internal NMOS transistor coupled to ground and to the first node;

a second internal NMOS transistor coupled to ground and to the second node;

a first pass NMOS transistor coupled to the first node; and

a second pass NMOS transistor coupled to the second node, wherein each transistor includes,

a substrate,

a bottom gate disposed on the substrate,

a high resistivity layer disposed on the substrate,

a channel disposed above the bottom gate,

a source disposed on the high resistivity layer and having a source extension extending from a main body of the source and coupled to the channel,

a drain disposed on the high resistivity layer and having a drain extension extending from a main body of the drain and coupled to the channel,

a gate insulator disposed on the channel,

a top gate disposed on the gate insulator,

a first insulating spacer disposed between the top gate and the source and proximate to the source extension,

a second insulating spacer disposed between the top gate and the drain and proximate to the drain extension,

a gate electrode including a local interconnect and coupled to the top gate,

wherein the gate electrode of the first internal PMOS transistor is coupled to the gate electrode of the first internal NMOS transistor and to the second node, and

wherein the gate electrode of the second internal PMOS transistor is coupled to the gate electrode of the second internal NMOS transistor and to the first node.

9. The SRAM cell of claim 8, wherein the channel of each transistor has a cross-sectional U-shape.

10. The SRAM cell of claim 9, wherein the gate insulator of each transistor has a cross-sectional U-shape.

11. The SRAM cell of claim 8 wherein each NMOS transistor further includes a second local interconnect insulated from the first local interconnect and coupled to the bottom gate and to ground.

12. The SRAM cell of claim 8 wherein each PMOS transistor further includes a second local interconnect insulated from the first local interconnect and coupled to the bottom gate and to Vdd.

13. The SRAM cell of claim 8 wherein the local interconnect of each transistor is insulated from the bottom gate.

14. The SRAM cell of claim 8, wherein the local interconnect of each transistor is coupled to the bottom gate.

15. The SRAM cell of claim 8, wherein the channel of each transistor is undoped.

16. The SRAM cell of claim 8, wherein the main body of the source and drain of each transistor is vertically disposed higher than the channel.

17. The SRAM cell of claim 8, wherein each transistor further includes a plurality of exterior spacers disposed on the substrate and proximate to the high resistivity layer, source, and drain.

18. The SRAM cell of claim 17, wherein each transistor further includes an insulator layer disposed on the substrate and coupled to the exterior spacers.

19. A SRAM cell, comprising:

a first internal PMOS transistor coupled to Vdd and a first node;

a second internal PMOS transistor coupled to Vdd and a second node;

a first internal NMOS transistor coupled to ground and to the first node; and

a second internal NMOS transistor coupled to ground and to the second node, wherein each transistor is double-gated with independent gate control and including,

a substrate,

a bottom gate disposed on the substrate,

a high resistivity layer disposed on the substrate,

a channel disposed above the bottom gate,

a source disposed on the high resistivity layer and having a source extension extending from a main body of the source and coupled to the channel,

a drain disposed on the high resistivity layer and having a drain extension extending from a main body of the drain and coupled to the channel,

a gate insulator disposed on the channel,

a top gate disposed on the gate insulator,

a first insulating spacer disposed between the top gate and the source and proximate to the source extension,

a second insulating spacer disposed between the top gate and the drain and proximate to the drain extension,

a first local interconnect coupled to the top gate and disposed between the first and second spacers, and

a second local interconnect insulated from the first local interconnect and coupled to the bottom gate,

wherein the first local interconnect of the first internal PMOS transistor is coupled to the first local interconnect of the first internal NMOS transistor and to the second node, and

wherein the first local interconnect of the second internal PMOS transistor is coupled to the first local interconnect of the second internal NMOS transistor and to the first node.

20. The SRAM cell of claim 19, wherein the channel of each internal transistor has a cross-sectional U-shape.

21. The SRAM cell of claim 19, wherein the gate insulator of each internal transistor has a cross-sectional U-shape.

22. The SRAM cell of claim 19, further comprising:

a first pass NMOS transistor coupled to the first node; and

a second pass NMOS transistor coupled to the second node.

23. The SRAM cell of claim 19, wherein the channel of each internal transistor is undoped.

24. The SRAM cell of claim 19, wherein the main body of the source and drain of each internal transistor is vertically disposed higher than the channel.

25. The SRAM cell of claim 19, wherein each internal transistor further includes a plurality of exterior spacers disposed on the substrate and proximate to the high resistivity layer, source, and drain.

26. The SRAM cell of claim 25, wherein each internal transistor further includes an insulator layer disposed on the substrate and coupled to the exterior spacers.

27. A radiation-resistant SRAM cell, comprising:

a first internal PMOS transistor coupled to Vdd and a first node;

a second internal PMOS transistor coupled to Vdd and a second node;

a first internal NMOS transistor coupled to ground and to the first node;

a second internal NMOS transistor coupled to ground and to the second node;

a first pass NMOS transistor coupled to the first node; and

a second pass NMOS transistor coupled to the second node, wherein each transistor includes,

a substrate,

a bottom gate disposed on the substrate,

a nitride dielectric disposed on the substrate,

a channel disposed above the bottom gate,

a source disposed on the nitride dielectric to prevent contact with the substrate, the source coupled to the channel,

a drain disposed on the nitride dielectric to prevent contact with the substrate, the drain coupled to the channel,

a gate insulator disposed on the channel,

a top gate disposed on the gate insulator,

a gate electrode including a local interconnect and coupled to the top gate, and

a plurality of nitride exterior spacers disposed on the substrate and surrounding the bottom gate, nitride dielectric, source, drain, gate insulator and top gate,

wherein the gate electrode of the first internal PMOS transistor is coupled to the gate electrode of the first internal NMOS transistor and to the second node, and

wherein the gate electrode of the second internal PMOS transistor is coupled to the gate electrode of the second internal NMOS transistor and to the first node.

28. The SRAM cell of claim 27 wherein each transistor further includes,

a first nitride pad disposed on the source; and

a second nitride pad disposed on the drain.

29. The SRAM cell of claim 28, wherein each transistor further includes,

a first contact extending through the first nitride pad and coupled to the source; and

a second contact extending through the second nitride pad and coupled to the drain.

30. The SRAM cell of claim 27, wherein, the source of each transistor includes a source extension extending from a main body of the source and coupled to the channel, and

the drain of each transistor includes a drain extension extending from a main body of the drain and coupled to the channel, and

wherein each transistor further includes,

a first insulating spacer disposed between the top gate and the source and proximate to the source extension, and

a second insulating spacer disposed between the top gate and the drain and proximate to the drain extension.

31. The SRAM cell of claim 27, wherein the channel of each transistor has a cross-sectional U-shape.

32. The SRAM cell of claim 31, wherein the gate insulator of each transistor has a cross-sectional U-shape.

33. The SRAM cell of claim 27, wherein each NMOS transistor further includes a second local interconnect insulated from the first local interconnect and coupled to the bottom gate and to ground.

34. The SRAM cell of claim 27, wherein each PMOS transistor further includes a second local interconnect insulated from the first local interconnect and coupled to the bottom gate and to Vdd.

35. The SRAM cell of claim 27, wherein the local interconnect of each transistor is insulated from the bottom gate.

36. The SRAM cell of claim 27, wherein the local interconnect of each transistor is coupled to the bottom gate.

37. The SRAM cell of claim 27, wherein the channel of each transistor is undoped.

38. A SRAM cell, comprising:

a first internal PMOS transistor coupled to Vdd and a first node;

a second internal PMOS transistor coupled to Vdd and a second node;

a first internal NMOS transistor coupled to ground and to the first node; and

a second internal NMOS transistor coupled to ground and to the second node, wherein each transistor is double-gated with independent gate control and including,

a bottom gate, and

a top gate, insulated from the bottom gate,

wherein the bottom gate of each NMOS transistor is coupled to ground,

wherein the top gate of the first internal PMOS transistor is coupled to the top gate of the first internal NMOS transistor and to the second node, and

wherein the top gate of the second internal PMOS transistor is coupled to the top gate of the second internal NMOS transistor and to the first node.

39. The SRAM cell of claim 38 further comprising:

a first pass NMOS transistor coupled to the first node and including a top gate and bottom gate, the bottom gate coupled to ground; and

a second pass NMOS transistor coupled to the second node and including a top gate and a bottom gate, the bottom gate coupled to ground.